ABSTRACT

The invention provides a process for fabricating a solid electrolytic capacitor of the chip type which process includes the steps of plating a fabrication frame comprising an anode terminal member and a cathode terminal member projecting from a pair of side frame members respectively so as to be opposed to each other, the anode terminal member being stepped so as to provide a lower portion toward the cathode terminal member, a hole extending vertically and being formed in each of the anode terminal member and a higher portion of the cathode terminal member, joining an anode lead of a capacitor element to an upper surface of the cathode terminal member and a bottom surface of the capacitor element to an upper surface of the lower portion of the cathode terminal member, forming a packaging resin portion around the capacitor element without permitting resin to ingress into the holes, and cutting the anode and cathode terminal members along vertical planes extending through the respective holes.